What is Claimed is:

1. A voltage generator comprising:

a detector for comparing an output voltage of the voltage generator with a first reference voltage and a second reference voltage lower than the first reference voltage to output a first sensing signal and a second sensing signal;

a controller for receiving the first sensing signal and the second sensing signal, and an action signal to output a first control signal and a second control signal;

a sub-booster for boosting a voltage in response to the first control signal;

a main booster for boosting a voltage in response to the second control signal; and

a voltage adder for adding output signals from the sub-booster and the main booster to provide the output voltage.

2. The voltage generator according to claim 1, wherein the detector comprises:

a sensing voltage generator for dividing the output voltage to generate a first sensing voltage and a second sensing voltage lower than the first sensing voltage;

a first comparator for comparing the first sensing voltage and the first reference voltage to output the first sensing signal; and

a second comparator for comparing the second sensing voltage and the

second reference voltage to output the second sensing signal.

3. The voltage generator according to claim 1, wherein the controller comprises:

an action detector for combining the first sensing signal and the second sensing signal, and the action signal to generate an output signal;

a latch for latching the output signal from the action detector; and

a sub-controller for receiving an output signal from the latch and the action signal to output the first control signal.

4. The voltage generator according to claim 3, wherein the sub-controller comprises:

a plurality of pulse generating blocks, each of which outputs a pulse in response to the action signal and the output signal from the latch; and

a multiplexer for selecting one pulse among a plurality of pulses in response to the action signal to output the one pulse as the first control signal.

5. The voltage generator according to claim 4, wherein the pulse generating block comprises:

a first operating means for performing a NAND operation on the output signal from the latch and the action signal;

an delay circuit for delaying an output signal from the first operating means for a predetermined time according to the action signal; and

a second operating means for performing a NAND operation on the

output signal from the first operating means and an output signal from the delay circuit to provide an output.

6. The voltage generator according to claim 1, wherein the main booster comprises:

an oscillator for outputting an oscillating signal in response to the second control signal;

a control driver for decoding the oscillating signal to output a plurality of capacitor precharge signals and a plurality of charge transport signals; and

a pump circuit for charging capacitors in response to the plurality of capacitor precharge signals and pumping charges stored in the capacitors in response to the plurality of charge transport signals to boost the output voltage.

7. The voltage generator according to claim 1, wherein the sub-booster comprises:

an oscillator for outputting an oscillating signal in response to the second control signal;

a control driver for decoding the oscillating signal to output a plurality of capacitor prechrage signals and a plurality of charge transport signals; and

a pump circuit for charging capacitors in response to the plurality of capacitor precharge signals and pumping charges stored in the capacitors in response to the plurality of charge transport signals to boost the output voltage.

8. The voltage generator according to claim 1, wherein

the detector further compares the output voltage with a third reference voltage greater than the first reference voltage to output a third sensing signal, and

the controller further receives the third sensing signal and the action signal to output a third control signal,

further comprising a second sub-booster for boosting a voltage in response to the third control signal, and wherein the voltage adder adds output signals from the sub-booster, the second sub-booster and the main booster to provide the output voltage.

9. A voltage generator comprising:

means for comparing an output voltage of the voltage generator with a first reference voltage and a second reference voltage lower than the first reference voltage to output a first sensing signal and a second sensing signal;

means for receiving the first sensing signal and the second sensing signal, and an action signal to output a first control signal and a second control signal;

means for boosting a voltage in response to the first control signal;

means for boosting a voltage in response to the second control signal; and

means for adding output signals from the sub-booster and the main booster to provide the output voltage.

10. The voltage generator according to claim 9, wherein the means for comparing further comprises:

means for dividing the output voltage to generate a first sensing voltage and a second sensing voltage lower than the first sensing voltage;

means for comparing the first sensing voltage and the first reference voltage to output the first sensing signal; and

means for comparing the second sensing voltage and the second reference voltage to output the second sensing signal.

11. The voltage generator according to claim 9, wherein the means for receiving further comprises:

means for combining the first sensing signal and the second sensing signal, and the action signal to generate an output signal;

means for latching the output signal from the action detector; and

means for receiving an output signal from the latch and the action signal to output the first control signal.

12. The voltage generator according to claim 11, wherein the means for receiving an output signal from the latch and the action signal further comprises:

means for generating a plurality of pulses each in response to the action signal and the output signal from the latch; and

means for selecting one pulse among a plurality of pulses in response to the action signal to output the one pulse as the first control signal.

13. The voltage generator according to claim 12, wherein the means for generating a plurality of pulses further comprises:

first operating means for performing a NAND operation on the output signal from the latch and the action signal to generate an output signal;

means for delaying an output signal from the first operating means for a predetermined time according to the action signal to generate an output signal; and

second operating means for performing a NAND operation on the output signal from the first operating means and the output signal from the means for delaying.

14. The voltage generator according to claim 9, wherein the means for boosting a voltage in response to the second control signal further comprises:

means for outputting an oscillating signal in response to the second control signal;

means for decoding the oscillating signal to output a plurality of capacitor precharge signals and a plurality of charge transport signals; and

means for charging capacitors in response to the plurality of capacitor precharge signals and pumping charges stored in the capacitors in response to the plurality of charge transport signals to boost the output voltage.

15. The voltage generator according to claim 9, wherein the means for boosting a voltage in response to the first control signal further comprises:

means for outputting an oscillating signal in response to the second control signal;

means for decoding the oscillating signal to output a plurality of capacitor prechrage signals and a plurality of charge transport signals; and

means for charging capacitors in response to the plurality of capacitor precharge signals and pumping charges stored in the capacitors in response to the plurality of charge transport signals to boost the output voltage.

16. A method for generating an output voltage with reduced noise, comprising:

receiving an action signal;

generating a first voltage signal in response to the action signal when the output voltage is less than a first reference voltage;

generating a second voltage signal in response to the action signal when the output voltage is less than a second reference voltage which is less than the first reference voltage; and

adding the first voltage signal and the second voltage signal to generate the output voltage.

17. The method for generating an output voltage with reduced noise according to claim 16, further comprising generating a third voltage signal in response to the action signal when the output voltage is less than a third reference voltage which is greater than the first reference voltage,

wherein the step of adding the first voltage signal and the second voltage

signal also adds the third voltage signal to generate the output voltage.

18. The method for generating an output voltage with reduced noise according to claim 16, further comprising:

dividing the output voltage to generate a first sensing voltage and a second sensing voltage lower than the first sensing voltage;

comparing the first sensing voltage and the first reference voltage and generate the first sensing signal in response thereto; and

comparing the second sensing voltage and the second reference voltage and generating the second sensing signal in response thereto.

19. A voltage generator comprising:

a first voltage sub-booster configured to provide a first voltage signal when the output voltage is less than a first reference voltage;

a main voltage booster configured to provide a second voltage signal when the output voltage is less than a second reference voltage that is less than the first reference voltage; and

a voltage adder configured to add the first voltage signal and the second voltage signal to provide the output voltage.

20. The voltage generator according to claim 19, further comprising a second voltage sub-booster configured to provide a third voltage signal when the output voltage is less than a third reference voltage which is greater than the first reference voltage, and wherein the voltage adder is configured to add the

first voltage signal, the second voltage signal and the third voltage signal to provide the output voltage.

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